A new ZVT-ZCT quasi-resonant DC link for soft switching inverters

S. Urgun, T. Erfidan, H. Bodur, B. Cakir

Civil Aviation College, Kocaeli University, Kocaeli, Turkey
Electrical Engineering Department, Kocaeli University, Kocaeli, Turkey
Electrical Engineering Department, Yildiz Technical University, Istanbul, Turkey

Online publication date: 04 January 2010

To cite this Article Urgun, S., Erfidan, T., Bodur, H. and Cakir, B.(2010) 'A new ZVT-ZCT quasi-resonant DC link for soft switching inverters', International Journal of Electronics, 97: 1, 83 — 97

To link to this Article: DOI: 10.1080/00207210903168322
URL: http://dx.doi.org/10.1080/00207210903168322

PLEASE SCROLL DOWN FOR ARTICLE
A new ZVT–ZCT quasi-resonant DC link for soft switching inverters

S. Urgun\textsuperscript{a,}\* T. Erfidan\textsuperscript{b}, H. Bodur\textsuperscript{c} and B. Cakir\textsuperscript{b}

\textsuperscript{a}Civil Aviation College, Kocaeli University, Kocaeli, Turkey; \textsuperscript{b}Electrical Engineering Department, Kocaeli University, Kocaeli, Turkey; \textsuperscript{c}Electrical Engineering Department, Yildiz Technical University, Istanbul, Turkey

\textit{(Received 3 November 2008; final version received 30 April 2009)}

In this article, the new ZVT–ZCT Quasi-Resonant DC Link, which ensures zero crossings at any time required for soft switching (SS) and provides zero voltage transition (ZVT) turn-on and zero current transition (ZCT) turn-off together for the main switch of active snubber cell in pulse width modulated or space vector modulated operation of inverter is presented. The new circuit combines the most desirable features of the circuits presented previously and overcomes most drawbacks of these circuits by using only one auxiliary switch with fewer other components. Consequently, new ZVT–ZCT Quasi-Resonant DC Link, which is verified by a prototype of a 1.2 kW and 50 kHz circuit, is analysed in detail. All semiconductor devices operate under SS, the main switch is subjected to no additional voltage and current stresses, and the stress on the auxiliary switch is very low in the proposed new inverter.

\textbf{Keywords:} soft switching; zero current transition; zero voltage transition; PWM inverter; quasi-resonant dc link

1. Introduction

The voltage source DC–AC converter has a large domain of applications, such as adjustable speed drives, uninterruptible power supplies, etc. In many of those applications the main advantage is the increasing of switching frequency. However, in hard-switching operations, switching losses increase with the switching frequency, which strongly reduces the power converter efficiency. For acceptable efficiency at higher switching frequencies, it is necessary to use fast semiconductors and drives to reduce rise and fall times of voltages (high \(dv/dt\)) (Monteiro and Anunciada 2002; Divan 1989).

Generally, a snubber circuit reduces the switching loss and switching stresses of the switches, but increases the total power loss in the converter. In recent years, various soft switching techniques have been proposed to reduce the switching losses and stresses without resorting to bulky and lossy passive snubbers. The term 'soft switching' means the device is only switched when the voltage across it and/or the current through it is zero. Thus there are two types of soft switching, zero voltage switching (ZVS) and zero current switching (ZCS). Various soft-switched dc–ac converters using either ZVS or ZCS have been proposed in the literature, and the

\*Corresponding author. Email: tarik@kocaeli.edu.tr
basic issue is to achieve high-frequency operation with reduced switching losses and electromagnetic interference (Divan 1989; Chen and Lipo 1996; Ballar et al. 1998; Yoshitsugu et al. 2001; Kurokawa et al. 2001; Behera et al. 2001; Shireen and Kulkarni 2003; Monteiro and Anunciada 2003; Abu-Qahouq and Batarsez 2002).

In recent years, several soft switching topologies have been proposed: Resonant DC Link (RDCL), Quasi Resonant DC Link, Passively Clamped Resonant DC Link, Actively Clamped Resonant DC Link (ACRL), Resonant DC Link with pulse width modulation (RDCL-PWM), Parallel Resonant DC Link (PRDCL) and Synchronized Resonant DC Link (SRDCL). However, the majority of the soft-switching topologies have some disadvantages, such as switch over voltage in RDCL and in SRDCL, the impossibility of using pulse width modulation (PWM) in RDCL and ACRL, increased losses and duty cycle limitations in RDCL-PWM, SRDCL and QRDCL, and control complexity in PRDCL and SRDCL (Monteiro and Anunciada 2002; Abu-Qahouq and Batarsez 2002).

Various schemes have been recently proposed for soft switching cells using two, three or four switches to achieve soft commutation for all main switches, auxiliary switches, and diodes, lower load ripple currents or lower total losses circuit complexity, control accuracy, minimal reactive energy storage and stress of components (Shireen and Kulkarni 2003; Monteiro and Anunciada 2003; Abu-Qahouq and Batarsez 2002; Jie Wu and Jiang 2004; Behera et al. 2004; Bodur and Bakan 2004; Obdan et al. 2005; Mandrek and Chrzan 2007). However in none of these recent works are both the ZVT turn-on and ZCT turn-off processes of the main switch used together.

In this article, a universal auxiliary circuit named Zero Current and Zero Voltage Transition (ZCZVT) commutation cell is applied to voltage source inverters (VSI). This topology presents one commutation cell for all legs. Figure 1(a) shows a ZCZVT full bridge inverter. As can be seen, the ZCZVT PWM commutation cell is placed between the DC source and the inverter.

With the use of the proposed commutation cell, which is activated only during the switching transitions, full load range soft switching for all power semiconductor devices is achieved. Furthermore, because of the limited $\frac{di}{dt}$ and $\frac{dv}{dt}$, main diode reverse recovery losses are minimised during the commutations, permitting the use of slower devices. Because the main switches commutate under zero current and zero voltage at both turn-on and turn-off, the ZCZVT commutation cell is suitable for both majority and minority carriers or semiconductor device applications such as

![Diagram](image.png)

Figure 1. New ZVT-ZCT quasi-resonant DC link inverter.
MOSFETs and IGBTs. This implies that this topology is suitable for a large range of output powers, where different semiconductor devices can be used.

The operation of the proposed ZCZVT commutation cell applied to a full-bridge PWM inverter is theoretically analysed in Section II. Section III presents the design procedure and Section IV presents the inverter features. The experimental results obtained from a 1.2 kW ZCZVT IGBT-based full-bridge inverter are given in Section V. Finally, Section VI summarises the conclusions drawn from this investigation.

2. Operation principles and analysis

2.1. Definitions and assumptions

The circuit scheme of new ZVT–ZCT Quasi-Resonant DC Link inverter is given in Figure 1. The proposed active snubber cell consists of a centre tapped and magnetic coupled snubber inductor ($L_{S1}$ and $L_{S2}$), a snubber capacitor ($C_S$), a resonant capacitor of $T_1$ ($C_r$), a main switch ($T_1$), an auxiliary switch ($T_2$), and two auxiliary diodes ($D_1$ and $D_2$). The diode $D_1$ can be considered as the body diode of the main switch. The parasitic capacitors of the semiconductor devices $T_1$, $D_2$ and $T_2$ are incorporated into the capacitor $C_r$, and are sufficient generally for the operation of the inverter. Thus, $C_r$ can be assumed to be the sum of these parasitic capacitors.

To simplify the steady state analysis of the circuit shown in Figure 1 during one switching cycle, it is assumed that input and output voltages and load current are constant, and semiconductor devices and resonant circuits are ideal. The reverse recovery time of the main diode is taken into account.

2.2. Operation stages

Ten stages occur over one switching cycle in the steady state operation of the proposed inverter. The equivalent circuit schemes of the operation stages are given in Figure 2(a)–(j), respectively, and key waveforms concerning these stages are shown in Figure 3. The detailed analysis of this inverter is presented as follows.

1) Stage 1 [$t_0 < t < t_1$: Figure 2(a)]: At the beginning of this stage, $i_{T1} = 0$, $i_{T2} = 0$, $i_{DF} = I_L$, $i_{CS} = i_{L_{S1}} = i_{L_{S2}} = 0$ and $V_{CS} = V_{C_{Smax2}}$ are valid. The main switch $T_1$ and the auxiliary switch $T_2$ are in the off-state, and the main diode $D_F$ is in the on state and conducts the load current $I_L$. At the moment a turn-on signal is applied to the gate of $T_2$ this stage begins. $T_2$ current rises and $D_F$ current falls simultaneously during this stage. The voltage of $V_{CS}$ decreases to $V_{CS}(t_2)$. For this stage, the equations;

\[ v_{CS}(t) = (V_i + V_{C_{Smax2}}) \cos(\omega_0(t - t_0)) - V_i \]  
\[ i_{L_{S2}}(t) = i_{CS}(t) = i_{T2}(t) = \frac{V_i + V_{C_{Smax2}}}{Z_0} \sin(\omega_0(t - t_0)) \]

are derived. At $t = t_1$, $i_{T2}$ reaches $I_L$ and $i_{DF}$ falls to 0 at $t_1$. Later $i_{DF}$ reaches $-I_{rr}$ at $t_2$ thus $D_F$ is turned off and this stage ends. Thus;

\[ i_{DF} = I_L - i_{L_{S2}}(t) = I_L - \frac{V_i + V_{C_{Smax2}}}{Z_0} \sin(\omega_0(t - t_0)) \]
Figure 2. Equivalent circuits of the operation stages in the proposed inverter.
Figure 3. Key waveforms concerning the operation stages in the proposed inverter.
\[ t_{01} = \frac{1}{\omega_0} \arcsin \left( \frac{I_L Z_0}{V_i + V_{C_{\text{max}}}^2} \right) \]  
\[ t_{12} = \frac{1}{\omega_0} \left[ \arcsin \left( \frac{(I_L + I_{rr}) Z_0}{V_i + V_{C_{\text{max}}}^2} \right) - \arcsin \left( \frac{I_L Z_0}{V_i + V_{C_{\text{max}}}^2} \right) \right] \]

can be written. Here \( I_{rr} \) and \( t_{rr} \) are the reverse recovery current and the reverse recovery time of \( D_F \), respectively. Therefore, \( T_2 \) is turned on with ZCS because of the \( L_{S2} \), and \( D_F \) is turned off with nearly ZCS and ZVS. In this state, the equations:
\[ \omega_0 = \frac{1}{\sqrt{L_{S2} C_S}} \]  
\[ Z_0 = \frac{\sqrt{L_{S2}}}{C_S} \]
are valid.

2) **Stage 2** \( [t_2 < t < t_3]: \) Figure 2(b): When \( i_{T1} = 0, \ i_{D_1} = 0, \ i_{T2} = i_{C_S} = i_{L_{S2}} = I_L + I_{rr}, V_{C_S} = V_{C_{S2}}(t_2) \) and \( V_{C_i} = V_i \) are existent at \( t = t_2 \) a resonance starts via the path \( T_2-C_S-L_{S2}-C_r \) under the load current \( I_L \). For this resonance:
\[ i_{L_{S2}} = i_{T_2} = i_{C_S} = (I_L + I_{rr}) \cos (\omega_0(t - t_2)) + \frac{V_{C_{S2}}}{Z_0} \sin (\omega_0(t - t_2)) \]  
\[ v_{C_S} = V_{C_{S2}} \cos (\omega_0(t - t_2)) - Z_0(I_L + I_{rr}) \sin (\omega_0(t - t_2)) \]
\[ t_{23} = \frac{1}{\omega_0} \cdot \arctan \left( \frac{V_{C_{S2}}}{Z_0(I_L + I_{rr})} \right) \]
\[ I_{L_{S_{\text{max}}}} = i_{L_{S2}}(t_3) = \sqrt{(I_L + I_{rr})^2 + \left( \frac{V_{C_{S2}}}{Z_0} \right)^2} \]  
\[ W_{L_{S_{\text{max}}}} = \frac{1}{2} L_{S2} \dot{i}_{L_{S_{\text{max}}}}^2 \]
are achieved. At \( t = t_3 \), \( v_{C_i} \) and \( v_{C_S} \) becomes 0 and this stage ends. Thus, the transfer of the energy stored in \( C_i \) to the inductor \( L_{S2} \) is completed. The current and energy values of the \( L_{S2} \) reach their maximum levels (\( I_{L_{S_{\text{max}}}} \)) at the same time.

3) **Stage 3** \( [t_3 < t < t_4]: \) Figure 2(c): Before \( i_{T1} = 0, \ i_{D_1} = 0, \ i_{T2} = i_{D_2} = i_{L_{S1}} = i_{L_{S2}} = I_{L_{S_{\text{max}}}}/2, \ v_{C_S} = 0 \) and \( V_{C_i} = 0 \) are valid. Just after \( v_{C_i} \) becomes 0 at \( t_3 \), the diode \( D_1 \) is turned on and this stage begins. \( D_1 \) conducts the excess of \( I_{L_{S_{\text{max}}}}/2 \) from \( I_L \) during this stage. The time period of this stage is the zero voltage transition (ZVT) time of the main switch. For this state:
\[ i_{L_{S1}} = i_{L_{S2}} = i_{T_2} = i_{D_2} = \frac{i_{L_{S_{\text{max}}}}}{2} \]
\[ i_{D_t} = \frac{i_{I_{S_{max}}} - I_L}{2} \]  
(14) 

\[ t_{34} : \text{selected} \]  
(15) 

can be written. At the instant the gate signal of \( T_2 \) is removed at \( t_4 \) this stage finishes. The turn-on signal of \( T_1 \) should be applied to its gate during ZVT.

4) Stage 4 \([t_4 < t < t_5]: \text{Figure 2(d)}\): At \( t = t_4 \), \( i_{T_1} = 0 \), \( i_{D_t} = 0 \), \( i_{T_2} = i_{D_2} = i_{L_{S1}} = i_{L_{S2}} = i_{I_{S_{max}}} \frac{2}{1} \), \( v_{C_t} = 0 \) and \( v_{C_S} = 0 \) are valid. As the gate signal of \( T_2 \) is removed at \( t_4 \), \( T_2 \) is turned off, \( T_1 \) is turned on and begins to conduct \( I_L \), and a resonance between the \( L_{S1} \) and \( C_S \) starts via the path \( D_2 - L_{S1} - C_S \). For this resonance;

\[ i_{L_{S1}} = i_{D_2} = i_{C_S} = I_{I_{S_{max}}} \cos (\omega_1 (t - t_4)) \]  
(16) 

\[ v_{C_S} = Z_1 I_{I_{S_{max}}} \sin (\omega_1 (t - t_4)) \]  
(17) 

\[ t_{45} = \frac{1}{\omega_1} \pi \]  
(18) 

are valid. At \( t_5 \), \( i_{L_{S1}} \) becomes 0, and thus this resonance and this stage are finished. Therefore, the energy stored in the snubber inductor is transferred to the snubber capacitor completely. The voltage value of \( C_S \) reaches its maximum level at this time. In this state, the equations;

\[ v_{C_S} (t_5) = V_{C_{S_{max}}} = Z_1 I_{I_{S_{max}}} \]  
(19) 

\[ W_{C_S} (t_5) = W_{C_{S_{max}}} = W_{L_{S1 \max}} = \frac{1}{2} C_S \cdot V_{C_{S_{max}}}^2 = \frac{1}{2} L_{S1} I_{C_{S_{max}}}^2 \]  
(20) 

are obtained. In these equations;

\[ \omega_1 = \frac{1}{\sqrt{L_{S1} C_S}} \]  
(21) 

\[ Z_1 = \sqrt{\frac{L_{S1}}{C_S}} \]  
(22) 

are existent. Therefore, the main switch \( T_1 \) is perfectly turned on under ZVS provided by ZVT, and the auxiliary switch is turned off under ZVS through the snubber capacitor in this stage.

5) Stage 5 \([t_5 < t < t_6]: \text{Figure 2(e)}\): This stage is the on state of inverter so the load is fed by the VSI via the main switch \( T_1 \). For this stage;

\[ i_{T_1} = I_L = I_i \]  
(23) 

can be written.

6) Stage 6 \([t_6 < t < t_7]: \text{Figure 2(f)}\): Before \( t = t_6 \), \( i_{T_1} = I_i = I_L \), \( i_{T_2} = i_{L_{S2}} = i_{L_{S1}} = i_{D_t} = 0 \) and \( v_{C_S} = V_{C_{S_{max}}} \) are existent. At \( t_6 \) as a turn-on signal is applied to
the gate of $T_2$, a resonance between $C_S$ and $L_{S2}$ starts via the path $T_2-C_S-L_{S2}-T_1$. During this stage, $T_2$ current rises and $T_1$ current falls simultaneously. At $t_7$, $T_2$ current reaches $I_L$ and $T_1$ current drops to zero, and this stage ends. The voltage of $V_{C_S}$ decreases to $V_{C_S}(t_7)$. The equations;

$$i_{T1} = I_L - i_{T2}$$

$$i_{L_{S2}} = i_{T2} = i_{C_S} = \frac{V_{C_{S\text{max}}}^{\text{S}}}{Z_0} \sin(\omega_0(t - t_7))$$

$$V_{C_S} = V_{C_{S\text{max}}}^{\text{S}} \cos(\omega_0(t - t_7))$$

$$t_{67} = \frac{1}{\omega_0} \arcsin\left(\frac{Z_0 I_L}{V_{C_{S\text{max}}}^{\text{S}}}\right) = \frac{1}{\omega_0} \arcsin\left(\frac{I_L}{I_{L_{S\text{max}2}}}\right)$$

are formed for this stage. Here $T_2$ is turned on with ZCS through $L_{S2}$.

7) **Stage 7** [$t_7 < t < t_8$: Figure 2(g)]: At the beginning of this stage, $i_{T1} = 0$, $i_{T2} = i_{L_{S2}} = i_{C_S} = I_L$ and $v_{C_S} = v_{C_S}(t_7)$ are valid. Just after $T_1$ current drops to zero at $t_7$, $D_1$ is turned on and this stage begins. During this stage, the resonance started before, continues via the path $T_2-C_S-L_{S2}-D_1$. At $t_8$ as $v_{C_S}$ falls to zero, the current and energy values of $L_{S2}$ reach their maximum levels ($I_{L_{S\text{max}2}}$), and this stage ends. For this stage;

$$i_{L_{S2}} = i_{T2} = i_{C_S} = \frac{V_{C_{S\text{max}}}^{\text{S}}}{Z_0} \sin(\omega_0(t + t_{67} - t_7))$$

$$v_{C_S} = V_{C_{S\text{max}}}^{\text{S}} \cos(\omega_0(t + t_{67} - t_7))$$

$$t_{78} = \frac{1}{\omega_0} \left(\frac{\pi}{2} - \arcsin\left(\frac{I_L}{I_{L_{S\text{max}2}}}\right)\right)$$

$$I_{L_{S\text{max}2}} = i_{L_{S2}}(t_8) = \frac{V_{C_{S\text{max}}}^{\text{S}}}{Z_0}$$

$$W_{L_{S\text{max}2}} = \frac{1}{2} L_{S2} I_{L_{S\text{max}2}}^2$$

are obtained. $D_1$ conducts the excess of $i_{L_{S2}}$ from $I_L$ during this stage.

8) **Stage 8** [$t_8 < t < t_9$: Figure 2(h)]: At $t_8$, $i_{T1} = 0$, $i_{T2} = i_{L_{S2}} = I_{L_{S\text{max}2}}/2$, $V_{C_S}$ = 0 and $v_{C_S} = 0$ existent. Just after $v_{C_S}$ becomes 0 at $t = t_8$ the diode $D_2$ is turned on and this stage begins. During this stage, $D_1$ conducts the excess of $I_{L_{S\text{max}2}}$ from $I_L$. The sum of the time periods of Stages 7 and 8, in which $D_1$ is in the on state, is the zero current transition (ZCT) time of $T_1$. For this stage;

$$i_{L_{S2}} = i_{L_{S1}} = i_{T2} = i_{D2} = \frac{I_{L_{S\text{max}2}}}{2}$$

$$i_{D1} = \frac{I_{L_{S\text{max}2}}}{2} - I_L$$
can be written. This stage finishes at the moment the gate signal of T₂ is removed at \( t_9 \). The turn-on signal of T₁ should be removed from its gate during ZCT.

9) Stage 9 \([ t_9 < t < t_{10} \): Figure 2(i)]: Before \( i_{T_1} = 0 \), \( i_{T_2} = i_{L_{S1}} = I_{L_{S1}max} \), \( i_{DF} = 0 \), \( v_{C_r} = 0 \) and \( v_{CS} = \) are existent. When the turn-on signal of T₂ is removed from its gate at \( t_9 \), T₂ is turned off and this stage starts. Two different closed circuits take place during this stage. \( C_r \) is charged by \( I_L \) linearly in the first circuit. A resonance between the \( L_{S1} \) and \( C_S \) begins via the path \( D_2-L_{S1}-C_S \) with the initial current \( I_{L_{S1}max} \) of \( L_{S1} \) in the other circuit. The voltage value of \( C_S \) reaches its maximum level \( (V_{C_{S,max}}) \) at this time. When \( i_{L_{S1}} \) current drops to zero this stage ends. The equations:

\[
i_{L_{S1}} = i_{D_2} = i_{C_S} = I_{L_{S1}max} \cos (\omega_1 (t - t_9))
\]

\[
v_{C_S} = Z_1 I_{L_{S1}max} \sin (\omega_1 (t - t_9))
\]

\[
V_{C_{S,max}} = v_{C_S}(t_{10}) = V_{C_{S10}} = Z_1 I_{L_{S1}max}
\]

are formed for this stage. The time period of this stage is derived as

\[
t_{910} = \frac{1}{\omega_1} \frac{\pi}{2}
\]

Therefore, the main switch T₁ is perfectly turned off under ZCS provided by ZCT, and the auxiliary switch T₂ is turned off under ZVS through the capacitors \( C_S \) and \( C_r \) in this stage.

10) Stage 10 \([ t_{10} < t < t_{11} \): Figure 2(j)]: This stage is the off-state of the inverter. For this stage;

\[
i_{T_1} = 0
\]

\[
i_{DF} = I_L
\]

can be written.

3. Design procedure

The detailed design procedure of the proposed new active snubber cell is mainly based on the ZVT turn-on and ZCT turn-off processes of the main switch. The new active snubber cell also provides soft switching for the other semiconductor devices in the inverter.

The following general comments about the operation of the new inverter are required to understand the design procedure and the features of the inverter, which are similarly mentioned
1. $C_r$ capacitor is accepted as a sum of main switch $T_1$ and other switches parasitic capacitors.

2. Coupled inductances $L_{S1}$ and $L_{S2}$ should be equal ($L_{S1} = L_{S2}$).

3. $V_{C_{S_{max1}}} = V_{C_{S_{max2}}}$, at steady state operation.

4. Equation (43) must be achieved to turn on auxiliary switch $T_2$ under soft switching condition.

\[
\frac{V_i + V_{C_{S_{max}}}}{L_{S2}} t_{rT2} \leq I_{L_{S_{max}}} \tag{43}
\]

Here, $t_{rT2}$ is the rise time of the auxiliary switch $T_2$.

5. Equation (44) must be achieved to turn off $D_F$ under soft switching condition.

\[
\frac{V_i + V_{C_{S_{max}}}}{L_{S2}} t_{rr} \leq I_{L_{S_{max}}} \tag{44}
\]

Here, $t_{rr}$ is the reverse recovery time of the main diode.

6. With reference to Figure. 3,

\[
t_{ZCT} = t_{78} + t_{89} \geq t_{fT1} \tag{45}
\]

can be written for the control conditions. Here, $t_{fT1}$ is the fall time of the main switch $T_1$.

7. To turn-on and turn-off of the main switch $T_1$ with ZVT and ZCT, respectively, $I_{L_{S_{max}}}$ should be selected as

\[
I_{L_{S_{max}}} \approx 3I_{L_{max}} \tag{46}
\]

8. To be limited voltage stresses on $T_2$ and $D_2$ with $2V_i$ ;

\[
V_{C_{S_{max}}} \leq \frac{V_i}{2} \tag{47}
\]

9. Operation stages intervals should be limited to minimum at component selection.

4. Inverter features

This new ZVT–ZCT Quasi-Resonant DC Link inverter equipped with the proposed active snubber cell combines most of the desirable features of both the ZVT and ZCT techniques, and overcomes most the drawbacks of inverters (Shireen and Kulkarni 2003; Monteiro and Anunciada 2003; Abu-Qahouq and Batarsez 2002; Jie Wu and Jiang 2004; Behera et al. 2004; Obdan et al. 2005; Mandrek and Chrzan 2007). The features of this new inverter can be briefly summarised as follows.

1. All semiconductor devices in this inverter operate under soft switching conditions. The main switch is both turned on with ZVT and turned off with
ZCT perfectly. The ZCS turn-on and the ZVS turn-off of the auxiliary switch are achieved. Also, the other devices operate with soft switching.

(2) The main switch $T_1$ and the main diode $D_F$ are not subjected to any additional voltage and current stresses. Moreover, the stresses on the auxiliary devices are very low.

(3) The soft switching operation of the new inverter is maintained for the whole line and load ranges.

(4) The inverter can operate at considerably high frequencies because load is supplied the resonant stages during most of the intervals.

(5) The new ZVT–ZCT Quasi-Resonant DC Link inverter ensures zero crossing on the DC link voltage at any time.

(6) The control signals of $T_1$ and $T_2$ of the proposed new active snubber cell can be obtained easily by PWM or SVM signals which are used by the inverter circuit.

(7) The new inverter is simpler and cheaper than most of the ZVT and ZCT converters presented previously. The proposed new active snubber cell can be easily applied to the other basic PWM and SVM inverters.

5. Implementation of circuit and experimental results

To verify the theoretical analysis of the proposed New ZVT–ZCT Quasi-Resonant DC Link inverter circuit, a prototype of a 1.2 kW and 50 kHz ZVT–ZCT Quasi-Resonant DC Link inverter, shown in Figure 1, was realised experimentally. The oscillograms given in Figures 4–5 were obtained from the operating circuit with Lecroy WaveSurfer6100 Oscilloscope. The design range of parameters and specifications selected for prototype applications are shown in Table 1.

In the oscillograms given in Figure 4, the switching signals of both $T_1$ and $T_2$ are seen.

![Figure 4](image)

Figure 4. Switching signals of $T_1$ and $T_2$ with 5 V/div and 1 $\mu$s/div.

![Figure 5](image)

Figure 5. Voltage and current of $T_1$ for SS with 100 V/div, 5 A/div and 1 $\mu$s/div.
From Figure 5, it can be mainly seen that T₁ operates entirely at soft switching conditions, no overlap between its voltage and current occurs, and so it has the only conduction loss. The anti-parallel diode D₁ of T₁ stays in an on-state for a very short time before T₁ is turned on and off, and so the ZVT turn-on and ZCT turn-off processes are perfectly realised.

In Figure 6, it is clearly seen that T₂ is switched in both ZVT and ZCT processes over one switching cycle. It is turned on under nearly ZCS, then conducts a current pulse with a short time, and at last turned off under nearly ZVS in both processes. The current pulse of T₂ in the ZVT process is greater than that in the ZCT process because of the reverse recovery current of D₇. The voltage stress on T₂ during the off-state of the inverter is \( V_i + V_{CS} \). However, in the on-state of the inverter only \( V_{CS} \) voltage is seen.

Figure 7 basically illustrates that D₇ is turned on and turned off under nearly ZCS and ZVS, respectively, and so its switching loss is very low. Both the main

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC input voltage/current</td>
<td>230 V/20 A</td>
</tr>
<tr>
<td>T₁</td>
<td>IXGH20N60UA1/IXYS</td>
</tr>
<tr>
<td>T₂</td>
<td>IXGH30N60B2/IXYS</td>
</tr>
<tr>
<td>D₂, D₇</td>
<td>BYT30P600/ST</td>
</tr>
<tr>
<td>Cₛ</td>
<td>50 nF/630 V</td>
</tr>
<tr>
<td>Lₛ₁, Lₛ₂</td>
<td>6.4 ( \mu )H</td>
</tr>
<tr>
<td>( I_L ) current source</td>
<td>50 ( \Omega )–600 ( \mu )H</td>
</tr>
</tbody>
</table>

Figure 6. Voltage and current of T₂ for SS with 100 V/div, 5 A/div and 1 \( \mu \)s/div.

Figure 7. Voltage and current of D₇ for SS with 100 V/div, 5 A/div and 1 \( \mu \)s/div.
devices $T_1$ and the main diode $D_F$ do not have any additional voltage and current stresses.

From Figure 8, it can be seen that $C_S$ is charged to a value of $\sim 1/2 V_i$ during the on-state and off-state of the inverter.

In Figure 9 the voltage and current waveforms of the main switch operating at hard switching conditions. From this figure, it can be seen that the main switch is turned on and the main diode is turned off with hard switching simultaneously, and also a short circuit by means of these main devices occurs at the same time. Also, the

![Figure 8. Voltage and current of $C_S$ for SS with 100 V/div, 5 A/div and 1 $\mu$s/div.](image1)

![Figure 9. Voltage and current of $T_1$ for HS at 50 kHz with 100 V/div, 5 A/div and 1 $\mu$s/div.](image2)

![Figure 10. Efficiency curves of the proposed SS and the HS converters compared.](image3)
main switch is turned off with hard switching. Very high losses occur in this hard switching case.

From Figure 10, it is seen that the overall efficiency of this new ZVT–ZCT Quasi-Resonant DC Link reaches a value over 98% at full output power of 1.2 kW and a switching frequency of 50 kHz with soft-switching cell where in hard switching case the overall efficiency was 93% (Obdan et al. 2005). It is also seen that the efficiencies at low output powers are relatively higher than most of the other soft-switched DC links. Because the new ZVT–ZCT Quasi-Resonant DC Link loss is dependent strongly on circulating energy generally, it is very low and also it becomes lower as the load current falls in the new converter.

Consequently, to provide SS and PWM operation of the inverters, the proposed new ZVT–ZCT Quasi-Resonant DC Link inverter circuit generates perfectly zero crossing on the DC link by using only one auxiliary switch. Finally, it was observed that all the experimental results exactly verified the theoretical analysis of the proposed new ZVT–ZCT Quasi-Resonant DC Link inverter.

6. Conclusion

In this study, a new ZVT–ZCT Quasi-Resonant DC Link inverter circuit is presented. This circuit provides zero crossings on the DC link to implement the SS and PWM operation of the inverters.

A new active snubber cell provides ZVT turn-on and ZCT turn-off together for the switches of the inverter and snubber cell semiconductors.

The new circuit combines the most desirable features of the circuits presented previously and overcomes most drawbacks of these circuits by using only one auxiliary switch with fewer amounts of other components.

Consequently, new ZVT–ZCT Quasi-Resonant DC Link inverter, which is verified by a prototype of a 1.2 kW and 50 kHz circuit, is analysed in detail. All semiconductor devices operate under soft switching, the main devices are subjected to no additional voltage and current stresses, and the stresses on the auxiliary devices are low in the proposed new inverter. Also, it has been seen that the efficiency of the proposed circuit is increased to about 98.2% from value of 97% in Obdan et al. (2005). Increase of this efficiency shows that semiconductors can operate with lower switching loss at high frequency. Increasing the overall system efficiency with a simpler topology presents the success of this study.

References


